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DATA SHEET

SAA4956TJ
2.9-Mbit field memory with noise reduction

Preliminary specification
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CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 QUICK REFERENCE DATA
5 BLOCK DIAGRAM
6 PINNING
7 FUNCTIONAL DESCRIPTION
7.1 Field memory function
7.1.1 Write operation
7.1.2 Read operation
7.1.3 Power-up and initialization
7.1.4 Old and new data access
7.1.5 Memory arbitration logic and self-refresh
7.1.6 Cascade operation
7.1.7 Test mode operation
7.2 Noise reduction function
7.2.1 Reformatting and formatting
7.2.2 Band-splitting
7.2.3 Motion detection
7.2.4 K-factor
7.2.5 Noise shape
7.3 I²C-bus interface
8 LIMITING VALUES
9 THERMAL CHARACTERISTICS
10 CHARACTERISTICS
11 APPLICATION INFORMATION
12 PACKAGE OUTLINE
13 SOLDERING
13.1 Introduction to soldering surface mount packages
13.2 Reflow soldering
13.3 Wave soldering
13.4 Manual soldering
13.5 Suitability of surface mount IC packages for wave and reflow soldering methods
14 DEFINITIONS
15 LIFE SUPPORT APPLICATIONS
16 PURCHASE OF PHILIPS I²C COMPONENTS

2.9-Mbit field memory with noise reduction SAA4956TJ

1 FEATURES

- 2949264-bit field memory with optional field based noise reduction
- 245772 × 12-bit organization
- 3.3 V power supply
- Inputs fully TTL compatible when using an extra 5 V power supply
- High speed read and write operations
- FIFO operations:
  - Full word continuous read and write
  - Independent read and write pointers (asynchronous read and write access)
  - Resettable read and write pointers.
- Optional field based noise reduction activated by an enable pin and controlled via the I²C-bus
- Optional random access by block function (40 words per block) enabled during pointer reset operation
- Quasi static (internal self-refresh and clocking pauses of infinite length)
- Write mask function
- Cascade operation possible
- Compatible with SAA4955TJ
- 16-Mbit CMOS DRAM process technology
- 40-pin SOJ package.

2 GENERAL DESCRIPTION

The SAA4956TJ is a 2949264-bit field memory with an optional field based noise reduction designed for advanced TV applications such as 100/120 Hz TV, PALplus, PIP and 3D comb filter. The SAA4956TJ is functional and pin compatible with the SAA4955TJ.

However, the SAA4956TJ has also, in addition to the field memory function, a field based noise reduction circuit. If this function is enabled it can be controlled via the I²C-bus.

The maximum storage depth is 245772 words × 12 bits. A FIFO operation with full word continuous read and write could be used as a data delay, for example. A FIFO operation with asynchronous read and write could be used as a data rate multiplier. Here the data is written once, then read as many times as required as long as new data is not written. In addition to the FIFO operations, a random block access mode is accessible during the pointer reset operation. When this mode is enabled, reading and/or writing may begin at, or proceed from, the start address of any of the 6144 blocks. Each block is 40 words in length. Two or more SAA4956TJs can be cascaded to provide a greater storage depth or a longer delay, without the need for additional circuitry.

The SAA4956TJ contains separate 12-bit wide serial ports for reading and writing. The ports are controlled and clocked separately, so asynchronous read and write operations are supported. Independent read and write clock rates are possible. Addressing is controlled by read and write address pointers. Before a controlled write operation can begin, the write pointer must be set to zero or to the beginning of a valid address block. Likewise, the read pointer must be set to zero or to the beginning of a valid address block before a controlled read operation can begin.

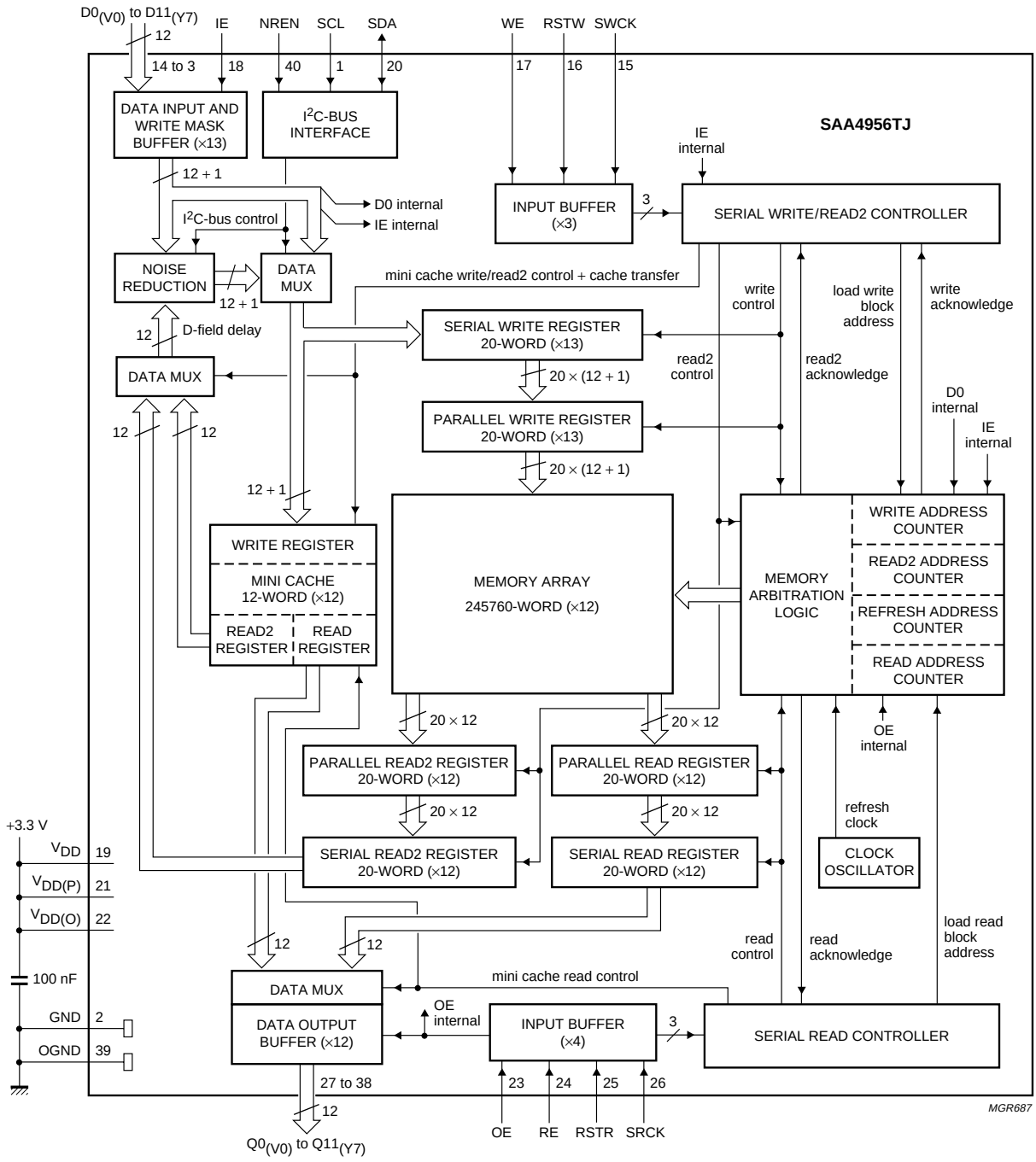
3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4956TJ	SOJ40	plastic small outline package; 40 leads (J-bent); body width 10.16 mm	SOT449-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$T_{cy(SWCK)}$	SWCK cycle time	NREN = LOW; see Fig.4	26	–	–	ns
		NREN = HIGH; see Fig.4	52	–	150	ns
$T_{cy(SRCK)}$	read cycle time (SRCK)	see Fig.11	26	–	–	ns
t_{ACC}	read access time after SRCK	see Fig.11	–	–	21	ns
V_{DD}	supply voltage (pin 19)		3.0	3.3	3.6	V
$V_{DD(O)}$	supply voltage (pin 22)		3.0	3.3	3.6	V
$V_{DD(P)}$	supply voltage (pin 21)		3.0	3.3	5.5	V
$I_{DD(tot)}$	total supply current ($I_{DD(tot)} = I_{DD} + I_{DD(O)} + I_{DD(P)}$)	minimum read/write cycle; outputs open	–	27	70	mA

5 BLOCK DIAGRAM



Pin 21 ($V_{DD(P)}$) should be connected to the supply voltage of the driving circuit that generates the input voltages. This could be, for instance, 5.0 V instead of 3.3 V. Pins 19 and 22 (V_{DD} and $V_{DD(O)}$) require a 3.3 V supply.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
SCL	1	digital input	serial clock of I^2C-bus
GND	2	ground	general purpose ground
$D11_{(Y7)}$	3	digital input	data input 11, Y input bit 7 if NREN is HIGH
$D10_{(Y6)}$	4	digital input	data input 10, Y input bit 6 if NREN is HIGH
$D9_{(Y5)}$	5	digital input	data input 9, Y input bit 5 if NREN is HIGH
$D8_{(Y4)}$	6	digital input	data input 8, Y input bit 4 if NREN is HIGH
$D7_{(Y3)}$	7	digital input	data input 7, Y input bit 3 if NREN is HIGH
$D6_{(Y2)}$	8	digital input	data input 6, Y input bit 2 if NREN is HIGH
$D5_{(Y1)}$	9	digital input	data input 5, Y input bit 1 if NREN is HIGH
$D4_{(Y0)}$	10	digital input	data input 4, Y input bit 0 if NREN is HIGH
$D3_{(U1)}$	11	digital input	data input 3, U input bits 1, 3, 5, 7 if NREN is HIGH
$D2_{(U0)}$	12	digital input	data input 2, U input bits 0, 2, 4, 6 if NREN is HIGH
$D1_{(V1)}$	13	digital input	data input 1, V input bits 1, 3, 5, 7 if NREN is HIGH
$D0_{(V0)}$	14	digital input	data input 0, V input bits 0, 2, 4, 6 if NREN is HIGH
SWCK	15	digital input	serial write clock
RSTW	16	digital input	write reset clock
WE	17	digital input	write enable
IE	18	digital input	input enable
V_{DD}	19	supply	3.3 V general purpose supply voltage
SDA	20	digital I/O	serial data of I^2C-bus
$V_{DD(P)}$	21	supply	3.3 to 5.5 V supply voltage for protection circuits
$V_{DD(O)}$	22	supply	3.3 V supply voltage for output circuits
OE	23	digital input	output enable
RE	24	digital input	read enable
RSTR	25	digital input	reset read
SRCK	26	digital input	serial read clock
$Q0_{(V0)}$	27	digital output	data output 0, V output bits 0, 2, 4, 6 if NREN is HIGH
$Q1_{(V1)}$	28	digital output	data output 1, V output bits 1, 3, 5, 7 if NREN is HIGH
$Q2_{(U0)}$	29	digital output	data output 2, U output bits 0, 2, 4, 6 if NREN is HIGH
$Q3_{(U1)}$	30	digital output	data output 3, U output bits 1, 3, 5, 7 if NREN is HIGH
$Q4_{(Y0)}$	31	digital output	data output 4, Y output bit 0 if NREN is HIGH
$Q5_{(Y1)}$	32	digital output	data output 5, Y output bit 1 if NREN is HIGH
$Q6_{(Y2)}$	33	digital output	data output 6, Y output bit 2 if NREN is HIGH
$Q7_{(Y3)}$	34	digital output	data output 7, Y output bit 3 if NREN is HIGH
$Q8_{(Y4)}$	35	digital output	data output 8, Y output bit 4 if NREN is HIGH
$Q9_{(Y5)}$	36	digital output	data output 9, Y output bit 5 if NREN is HIGH
$Q10_{(Y6)}$	37	digital output	data output 10, Y output bit 6 if NREN is HIGH
$Q11_{(Y7)}$	38	digital output	data output 11, Y output bit 7 if NREN is HIGH
OGND	39	ground	ground for output circuits
NREN	40	digital input	noise reduction enable

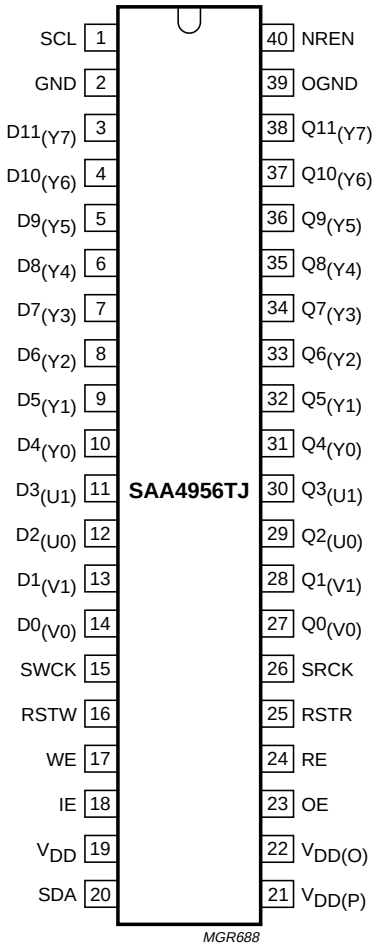


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The functional description is divided into 3 main sections:

- The basic field memory function (see Section 7.1)
- The optional noise reduction function (used in case the NREN signal is HIGH; see Section 7.2)
- The I^2C-bus interface function (which controls the noise reduction circuit; see Section 7.3).

7.1 Field memory function

The basic field memory function is fully compatible with the SAA4955TJ if the NREN signal is LOW. In this case the noise reduction function is bypassed via a data mux. If the NREN signal is HIGH the basic field memory function can only be executed with a write frequency restricted to half of the read operation frequency. In this case the random block access modes are not supported because a second read operation (READ2) is activated with an identical frequency as used in the write operations. The PAN-IC (SAA4995WP) needs approximately the same write frequency for the noise reduction option as the read frequency (32 MHz). To allow this configuration the self-refresh must be switched off via the I^2C-bus interface.

7.1.1 WRITE OPERATION

Write operations are controlled by the SWCK, RSTW, WE and IE signals. A write operation starts with a reset write address pointer (RSTW) operation, followed by a complete cycle of the SWCK clock during which time WE and IE must be held HIGH. Write operations between two successive reset write operations must contain at least 40 SWCK write clock cycles while WE is HIGH. To transfer data temporarily stored in the serial write registers to the memory array, a reset write operation is required after the last write operation.

7.1.1.1 Reset write: RSTW

The first positive transition of SWCK after RSTW goes from LOW-to-HIGH resets the write address pointer to the lowest address (–12 decimal), regardless of the state of WE (see Figs 4 and 5). RSTW set-up ($t_{su(RSTW)}$) and hold ($t_{h(RSTW)}$) times are referenced to the rising edge of SWCK (see Fig.4). The reset write operation may also be asynchronously related to the SWCK signal if WE is LOW.

RSTW needs to stay LOW for a single SWCK cycle before another reset write operation can take place. If RSTW is HIGH for 1024 SWCK write clock cycles while WE is HIGH, the SAA4956TJ will enter a built-in test mode.

7.1.1.2 Random write block access mode

The SAA4956TJ will enter random write block access mode if the following signal sequence is applied to control inputs IE and WE during the first four SWCK write clock cycles after a reset write (see Figs 6 and 7):

1. At the 1st and 2nd positive transitions of SWCK, IE must be LOW and WE must be HIGH
2. At the 3rd and 4th positive transitions of SWCK, IE must be HIGH and WE must be LOW
3. At the 5th positive transition of SWCK, the state of WE determines which input pin is used for the block address. If WE is LOW the Most Significant Bit (MSB) of the block address must be applied to the D0 input pin. If WE is HIGH, the MSB of the block address is applied to pin IE.

During this time, control signals WE and IE will function as defined for normal operation. The remaining 12 bits of the 13-bit write block address must be applied, in turn, to the selected input pin (D0 or IE) at the following 12 positive transitions of SWCK. The Least Significant Bit (LSB) of the write block address is applied at the 17th positive transition of SWCK. A write latency period of 18 additional SWCK clock cycles is required before write access to the new block address is possible. During this time, data is transferred from the serial write and parallel write registers into the memory array and the write pointer is set to the new block address.

Block address values between 0 and 6143 are valid. Values outside this range must be avoided because invalid block addresses can result in abnormal operation or a lock-up condition. Recovery from lock-up requires a standard reset write operation.

WE must remain LOW from the 3rd positive transition of SWCK to the 17th write latency SWCK clock cycle if the block address is applied to pin D0. If the block address is applied to pin IE, WE must be HIGH on the 5th positive transition of SWCK, may be HIGH or LOW on the 6th transition, and must be LOW from the 7th transition to the 17th write latency SWCK clock cycle.

At the 18th write latency SWCK clock cycle, IE and WE may be switched HIGH to prepare for writing new data at the next positive transition of SWCK. The complete write block access entry sequence is finished after the 18th write latency cycle.

The LOW-to-HIGH transition on RSTW required at the beginning of the sequence should not be repeated. Additional LOW-to-HIGH transitions on RSTW would disable write block address mode and reset the write pointer.

7.1.1.3 Address organization

Two different types of memory are used in the data address area: a mini cache for the first 12 data words after a reset write or a reset read, and a DRAM cell memory array with a 245760 word capacity. Each word is 12 bits long. The mini cache is needed to store data temporarily after a reset operation since a latency period is required before read or write access to the memory array is possible. Latency periods are needed for read or write operations in random read or write block access modes because data is read from, or written to, the memory array. The data in the mini cache can only be accessed directly after a standard reset operation. It cannot be accessed in random read or write block access modes.

The address area reserved for the mini cache, accessible after a standard reset operation, is from decimal −12 to −1. The memory array starts at decimal 0 and ends at 245759. Decimal address 0 is identical to block address 0000H. Because a single block address is defined for every 40 words in the memory array, block address 0001H corresponds to decimal address 40. The highest block address is 17FFH. This block has a decimal start address of 245720 and an end address of 245759.

If a read or write reset operation is not performed, the next read or write pointer address after 245759 will be address 0 due to pointer wraparound. It should be noted that reset read and write operations should occur together. If one pointer wraps around while the other is reset, either 12 words will be lost or 12 words of undefined data will be read.

7.1.1.4 Data inputs: D0 to D11 and write clock: SWCK

A positive transition on the SWCK write clock latches the data on inputs D0 to D11, provided WE was HIGH at the previous positive transition of SWCK. The data input set-up ($t_{su(D)}$) and hold ($t_{h(D)}$) times are referenced to the positive transition of SWCK (see Fig.5). The latched data will only be written into memory if IE was HIGH at the previous positive transition of SWCK.

7.1.1.5 Write enable: WE

Pin WE is used to enable or disable a data write operation. The WE signal controls data inputs D0 to D11. In addition, the internal write address pointer is incremented if WE is HIGH at the positive transition of the SWCK write clock. WE set-up ($t_{su(WE)}$) and hold ($t_{h(WE)}$) times are referenced to the positive edge of SWCK (see Fig.8).

7.1.1.6 Input enable: IE

Pin IE is used to enable or disable a data write operation from the D0 to D11 data inputs into memory. The latched data will only be written into memory if the IE and WE signals were HIGH during the previous positive transition of SWCK. A LOW level on IE will prevent the data being written into memory and existing data will not be overwritten (write mask function; see Fig.10). The IE set-up ($t_{su(IE)}$) and hold ($t_{h(IE)}$) times are referenced to the positive edge of SWCK (see Fig.9).

7.1.2 READ OPERATION

Read operations are controlled by the SRCK, RSTR, RE and OE signals. A read operation starts with a reset read address pointer (RSTR) operation, followed by a complete cycle of the SRCK clock during which time RE and OE must be held HIGH. Read operations between two successive reset read operations must contain at least 20 SRCK read clock cycles while RE is HIGH.

7.1.2.1 Reset read: RSTR

The first positive transition of SRCK after RSTR goes from LOW-to-HIGH resets the read address pointer to the lowest address (–12 decimal; see Figs 11 and 12). If RE is LOW, however, the reset read operation to the lowest address will be delayed until the first positive transition of SRCK after RE goes HIGH. RSTR set-up ($t_{su(RSTR)}$) and hold ($t_{h(RSTR)}$) times are referenced to the rising edge of SRCK (see Fig.11). The reset read operation may also be asynchronously related to the SRCK signal if RE is LOW.

RSTR needs to stay LOW for a single SRCK cycle before another reset write operation can take place.

7.1.2.2 Random read block access mode

The SAA4956TJ will enter random read block access mode if the following signal sequence is applied to control inputs RE and OE during the first four SWCK write clock cycles after a reset read (see Fig.13):

1. At the 1st and 2nd positive transitions of SRCK, OE must be LOW and RE must be HIGH
2. At the 3rd and 4th positive transitions of SRCK, OE must be HIGH and RE must be LOW.

During this time, control signals RE and OE will function as defined for normal operation. The Most Significant Bit (MSB) of the block read address is applied to the OE input pin at the 5th positive transition of SRCK. The remaining 12 bits of the 13-bit read block address must be applied, in turn, to OE at the following 12 positive transitions of SWCK. The Least Significant Bit (LSB) of the block address is applied at the 17th positive transition of SRCK. A read latency period of 20 additional SRCK clock cycles is required before read access to the new block address is possible. During this period, data is transferred from the memory array to the serial read and parallel read registers and the read pointer is set to the new block address.

Block address values between 0 and 6143 are valid. Values outside this range must be avoided because invalid block addresses can result in abnormal operation or a lock-up condition. Recovery from lock-up requires a standard reset read operation.

The data output pins are not controlled by the OE pin and are forced into high impedance mode from the 3rd to the 17th positive transition of SRCK. OE should be held LOW during the read latency period. RE must remain LOW from the 3rd positive transition of SRCK to the 20th read latency SRCK clock cycle.

After the 20th read latency SRCK clock cycle, RE and OE may be switched HIGH to prepare for reading new data from the new address block at the next positive transition of SRCK. The complete read block access entry sequence is finished after the 20th read latency cycle.

The LOW-to-HIGH transition on RSTR required at the beginning of the sequence should not be repeated. Additional LOW-to-HIGH transitions on RSTR would disable the read block address mode and reset the read pointer.

7.1.2.3 Data outputs: Q0 to Q11 and read clock: SRCK

The new data is shifted out of the data output registers on the rising edge of the SRCK read clock provided RE and OE are HIGH. Data output pins are low impedance if OE is HIGH. If OE is LOW, the data outputs are high impedance and the data output bus may be used by other devices. Data output hold ($t_{h(Q)}$) and access times (t_{ACC}) are referenced to the positive transition of SRCK. The output data becomes valid after access time interval t_{ACC} (see Fig.12).

Data output pins Q0 to Q11 are TTL compatible with the restriction that when the outputs are high impedance, they must not be forced higher than $V_{DD(O)}$ + 0.5 V or 5.0 V absolute. The output data has the same polarity as the incoming data at inputs D0 to D11.

7.1.2.4 Read enable: RE

RE is used to increment the read pointer. Therefore, RE needs to be HIGH at the positive transition of SRCK. When RE is LOW, the read pointer is not incremented. RE set-up ($t_{su(RE)}$) and hold times ($t_{h(RE)}$) are referenced to the positive edge of SRCK (see Fig.14).

7.1.2.5 Output enable: OE

OE is used to enable or disable data outputs Q0 to Q11. The data outputs are enabled (low impedance) if OE is HIGH. OE LOW disables the data output pins (high impedance). Incrementing of the read pointer does not depend on the status of OE. OE set-up ($t_{su(OE)}$) and hold times ($t_{h(OE)}$) are referenced to the positive edge of SRCK (see Fig.15).

7.1.3 Power-up and initialization

Reliable operation is not guaranteed until at least 100 μs after power-up, the time needed to stabilize V_{DD} within the recommended operating range. After the 100 μs power-up interval has elapsed, the following initialization sequence must be performed: a minimum of 12 dummy read operations (SRCK cycles) followed by a reset read operation (RSTR), and a minimum of 12 dummy write operations (SWCK) followed by a reset write operation (RSTW). Read and write initialization may be performed simultaneously.

If initialization starts earlier than the recommended 100 μs after power-up, the initialization sequence described above must be repeated, starting with an additional reset read operation and an additional reset write operation after the 100 μs start-up time.

7.1.4 Old and new data access

A minimum delay of 40 SWCK clock cycles is needed before newly written data can be read back from memory (see Fig.16). If a reset read operation (RSTR) occurs in a read cycle before a reset write operation (RSTW) in a write cycle accessing the same location, then old data will be read.

Old data will be read provided a data read cycle begins within 20 pointer positions of the start of a write cycle. This means that if a reset read operation begins within 20 SWCK clock cycles after a reset write operation, the internal buffering of the SAA4956TJ will ensure that old data will be read out (see Fig.17).

New data will be read if the read pointer is delayed by 40 pointer positions or more after the write pointer. Old data is still read out if the write pointer is less than or equal to 20 pointer positions ahead of the read pointer (internal buffering). A write pointer to read pointer delay of more than 20 but less than 40 pointer positions should be avoided. In this case, the old or the new data may be read, or a combination of both.

In random read and write block access modes, the minimum write-to-read new data delay of 40 SWCK clock cycles must be inserted for each block.

7.1.5 Memory arbitration logic and self-refresh

Since the data in the memory array is stored in DRAM cells, it needs to be refreshed periodically. Refresh is performed automatically under the control of internal memory arbitration logic which is clocked by a free running clock oscillator. The memory arbitration logic controls memory access for read, write and refresh operations. It uses the contents of the write, read and refresh address counters to access the memory array to load data from the parallel write register, store data in the parallel read register, or to refresh stored data. The values in these counters correspond to block addresses.

7.1.6 Cascade operation

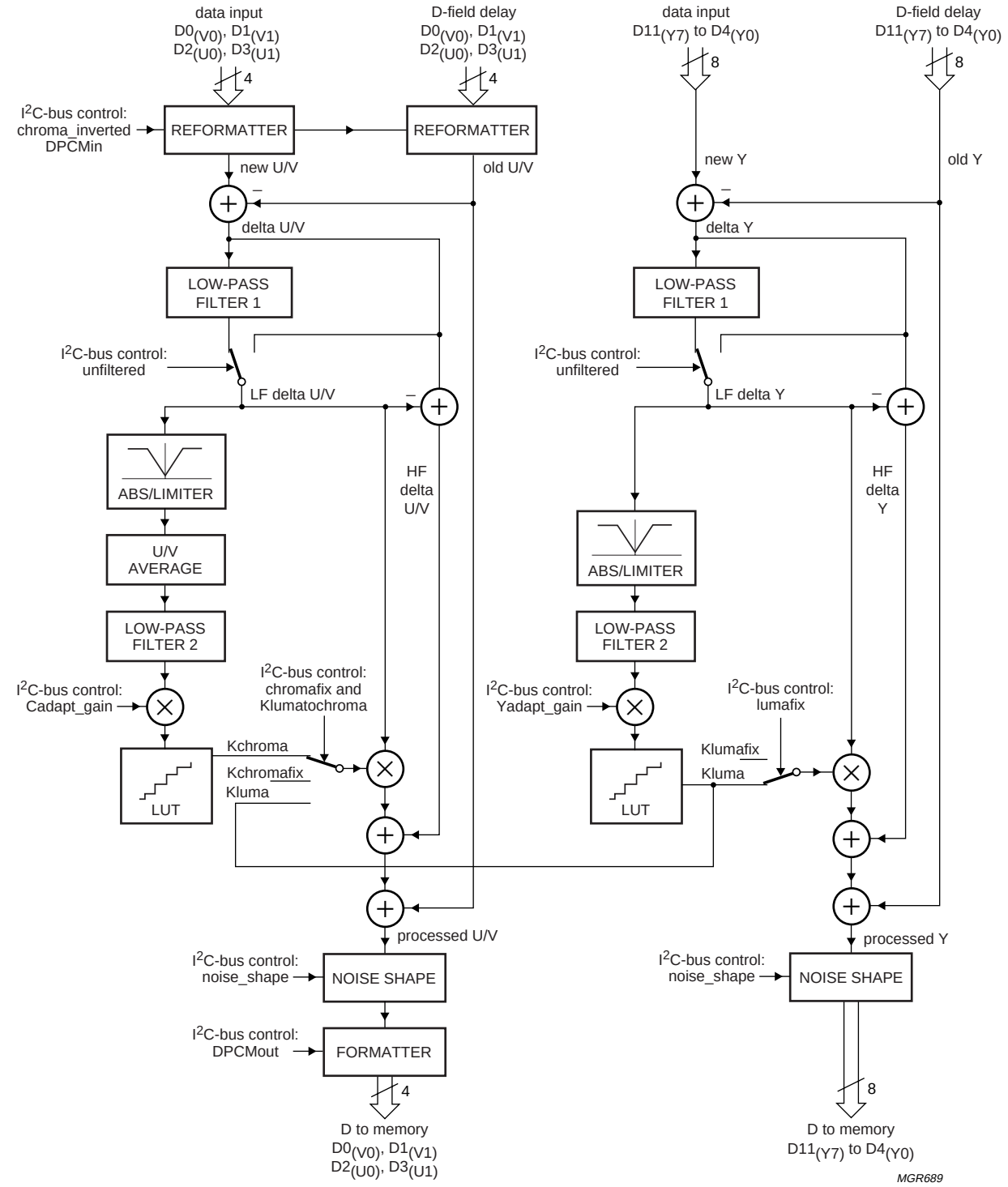
If a longer delay is needed, the total storage depth can be increased beyond 2949264 bits by cascading several SAA4956TJs. For details see the interconnection and timing diagrams (Figs 18 and 19).

The noise reduction function can be realized by enabling this function with the NREN pin at one of the cascaded SAA4956TJs.

7.1.7 Test mode operation

The SAA4956TJ incorporates a test mode not intended for customer use. If WE and RSTW are held HIGH continuously for 1024 SWCK clock cycles, the SAA4956TJ will enter test mode. It will exit test mode if WE is LOW for a single SWCK cycle or if RSTW is LOW for 2 SWCK clock cycles.

7.2 Noise reduction function



Switch position is off.

Fig.3 Block diagram of noise reduction.

The main function of the noise reduction is shown in Fig.3. It is divided in two signal paths for chrominance and luminance. Two operating modes can be used in principal: the fixed and the adaptive mode. In both modes the applied frequency range, where the noise reduction takes place, can be reduced or not reduced (I^2C-bus control: unfiltered).

The noise reduction operates field recursive with an average ratio between fresh (new) and over previous fields averaged (old) luminance and chrominance. Noise reduction can be activated by forcing the NREN control signal to HIGH. In this case the system starts with default settings for noise reduction and noise shape, if clock is applied to SWCK. If NREN is LOW the noise reduction block is bridged via a data mux (see Fig.1). During NREN HIGH, only half of the write frequency, which is allowed during NREN LOW, can be applied. This is explained by the need for a second memory read access (READ2) to get old data (D-field delay) in the same frequency as the write frequency. The noise reduction is controlled via I^2C-bus settings. Since the PAN-IC (SAA4995WP) needs approximately the same write frequency as the read frequency for the noise reduction option (32 MHz), a deactivated self-refresh is required. This setting can be done via the I^2C-bus interface (I^2C-bus control: no_refresh).

In the fixed mode, the noise reduction produces a constant weighted input averaging. Because of smearing effects this mode should not be used for normal operation except for K = 1. The fixed mode can be activated separately for chrominance (I^2C-bus control: chromafix) and luminance (I^2C-bus control: lumafix).

In the adaptive mode, the averaging ratio (K-factor) is based on the absolute differences of luminance respectively chrominance among the inputs. When the absolute difference is low, only a small part of the fresh data will be added. In cases of high difference, much of fresh data will be taken. This occurs in either situation of movement or where a significant vertical contrast is seen. The relation between the amount of movement and the K-factor values is defined via a Look-Up Table (LUT) where the steps can be programmed (I^2C-bus controls: Ksteps).

It should be noted that recursion is done over fields, and that pixel positions between the new and old fields always have a vertical offset of one line. So averaging is not only done in the dimension of time but also in the vertical direction. Therefore averaging vertically on e.g. a vertical black to a white edge would provide a grey result.

The averaging in chrominance can be slaved optionally to the luminance averaging (I^2C-bus control: Klumatochroma), therefore chrominance differences are not taken into account for the K-factor setting of the chrominance signal path.

The noise reduction scheme effectively also decreases the cross-colour patterns if for the averaging in chrominance the adaptive noise reduction is slaved to the luminance averaging (I^2C-bus control: Klumatochroma).
The cross-colour pattern does not produce an increase of the measured luminance difference, therefore this pattern will be averaged over many fields.

7.2.1 Reformatting and formatting

The standard applications are using the 4 : 1 : 1 YUV data stream (see Table 1). The noise reduction processing uses internally the 4 : 2 : 2 data stream. An up converter to 4 : 2 : 2 is applied with a linear interpolation filter for creation of the extra samples. These are combined with the original samples from the 4 : 1 : 1 stream. Instead of the 4 : 1 : 1 mode the input or output colour can be handled as DPCM format which is a certain data compression (I^2C-bus control: DPCMin, DPCMout) if the 4 : 2 : 2 data bandwidth is needed e.g. for applications together with SAA4978H. The incoming colour data can be also inverted for special purposes (I^2C-bus control: Chroma_inverted).

Table 1 Digital input and output bus format

4 : 1 : 1 FORMAT				**INPUT PIN**
Y07	Y17	Y27	Y37	$D11_{(Y7)}$
Y06	Y16	Y26	Y36	$D10_{(Y6)}$
Y05	Y15	Y25	Y35	$D9_{(Y5)}$
Y04	Y14	Y24	Y34	$D8_{(Y4)}$
Y03	Y13	Y23	Y33	$D7_{(Y3)}$
Y02	Y12	Y22	Y32	$D6_{(Y2)}$
Y01	Y11	Y21	Y31	$D5_{(Y1)}$
Y00	Y10	Y20	Y30	$D4_{(Y0)}$
U07	U05	U03	U01	$D3_{(U1)}$
U06	U04	U02	U00	$D2_{(U0)}$
V07	V05	V03	V01	$D1_{(V1)}$
V06	V04	V02	V00	$D0_{(V0)}$

The start position, when the first phase of the 4 : 1 : 1 YUV data word is expected on the input bus, is defined by the first valid written or read word after a reset write or a reset read operation. The luminance input signal is expected in 8-bit straight binary format, whereas U and V input signals are expected in twos complement format. U and V input signals are inverted if the corresponding I²C-bus control bit chroma_invert is set to logic 1.

7.2.2 BAND-SPLITTING

After reformatting, the frequencies of the difference signals of luminance (delta Y) and chrominance (delta U/V) can be divided optionally in an upper band (HF) and lower band (LF) with a lowpass-filter in both signal paths. The lower frequency band signals (LF delta Y and LF delta U/V) will be used as input for the noise reduction function. The lower frequency band on these signals means that the specific picture contents does not move or is moving slowly. Optionally, it is possible to bridge the band-splitting (I²C-bus control: unfiltered = 1).

7.2.3 MOTION DETECTION

The same signals, on which the noise reduction will be applied, are used to detect the amount of motion in the difference signals. Therefore, the absolute value of the difference signals are generated and limited to a maximum value. Afterwards the absolute values of the difference signal of U and V are averaged. The signals are low-pass filtered to smooth these signals. The filtered signals are amplified, depending on the setting of the I²C-bus controls: Yadapt_gain respectively Cadapt_gain (see Table 2).

Table 2 Gain settings of adaptive values for chrominance and luminance

Yadapt_gain/Cadapt_gain[2 to 0]		GAIN
HEX	DECIMAL	
00	00	$^{1}/_{8}$
01	01	$^{2}/_{8}$
02	02	$^{4}/_{8}$
03	03	$^{8}/_{8}$
04	04	$^{16}/_{8}$
05	05	$^{32}/_{8}$
06	06	$^{64}/_{8}$
07	07	$^{128}/_{8}$

The amplified signals, which correlate to the amount of movement in the chrominance respectively luminance signal path, are transferred into 1 out of 16 possible K-factor values via look-up tables. The K-factor values are defined by step values of the look-up tables. The step values are programmed via the I²C-bus-controls: Kstep0 to Kstep7 (see Table 3). These values are valid for the look-up tables of the chrominance and the luminance. For example, Kstep3 = 4 means: values which are smaller than 8 (4 times weight of 2) are at least K = $^{3}/_{8}$ or smaller and values equal or higher than 8 are at least K = $^{4}/_{8}$ or higher.

7.2.4 K-FACTOR

The amount of noise reduction (field averaging) is described via the K-factor. K = 1 means that no averaging is applied and the new field information is used. K = 0 means that no averaging is applied and thus only the old field information is used like a still picture mode. All values in between mean that a weighted averaging is applied. It is possible to use fixed K-factor values if the I²C-bus variable lumafix respectively chromafix is set to logic 1.
The possible fixed K-factor values of the I²C-bus control variables Klumafix and Kchromafix are described in Table 3.

Table 3 Settings of fixed K-factor values

Klumafix/Kchromafix[3 to 0]		K-factor
HEX	DECIMAL	
00	00	0
01	01	$^{1}/_{16}$
02	02	$^{2}/_{16}$
03	03	$^{3}/_{16}$
04	04	$^{4}/_{16}$
05	05	$^{5}/_{16}$
06	06	$^{6}/_{16}$
07	07	$^{7}/_{16}$
08	08	$^{8}/_{16}$
09	09	$^{9}/_{16}$
0A	10	$^{10}/_{16}$
0B	11	$^{11}/_{16}$
0C	12	$^{12}/_{16}$
0D	13	$^{13}/_{16}$
0E	14	$^{14}/_{16}$
0F	15	$^{16}/_{16}$

7.2.5 NOISE SHAPE

If the noise shaping is activated possible shadow picture information in the chrominance and the luminance path, resulting from a low K-factor value, will be eliminated. The noise shaping function can be switched off by means of the I²C-bus control. Subregister noise_shape = 0 is applied to show the effect.

7.3 I²C-bus interface

The I²C-bus interface in the SAA4956TJ is used in a receive mode. The standardized bus frequencies of both 100 kHz and 400 kHz can be dealt with.

As a slave receiver, the SAA4956TJ provides 8 registers for storing commands and data. These registers are accessed via so-called subaddresses. A subaddress can be thought of as a pointer to an internal memory location.

It is allowed to send one data byte or more data bytes per transmission to the SAA4956TJ. In this event, the subaddress is automatically incremented after each data byte, resulting in storing the sequence of data bytes at successive register locations, starting at SUBADDRESS. A transmission can start at any valid subaddress. Each data byte is acknowledged with ACK (acknowledge).

There is no ‘wrap around’ of subaddresses. Commands and data are processed as soon as they have been completely received. Data patterns sent to the various subaddresses are not checked for being illegal or not at that address. Detection of a STOP condition without a preceding acknowledge bit is regarded as a bus error. The last operation will not then be executed. Invalid subaddresses are not acknowledged.

The default I²C-bus settings can be loaded by changing the state of the NREN pin from LOW to HIGH during clocking of the SWCK and SCL pins. This can be realized for example by delaying the NREN signal with an RC-circuit for 1 second during the power-up sequence. This is necessary to give the circuit a minimum of 20 cycles of SCL and 100 cycles of SWCK after all input signals are stabilized.

Table 4 I²C-bus control; slave address, subaddress and data format

S	SLAVE ADDRESS	0	ACK	SUBADDRESS	ACK	DATA	ACK	...	DATA	ACK	P

Table 5 Description of bits used in Table 4

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address: 1011 111 (last bit is LSB)
0	data direction bit (write to device)
ACK	acknowledge
SUBADDRESS	address of register to write to
DATA	data byte to be written into register
P	STOP condition

Table 6 Write registers

REGISTER	BIT	NAME	DEFAULT	FUNCTION
Subregister 20H to 23H (Ksteps of the look-up tables of luminance and chrominance)				
20H	0 to 3	Kstep0	2	step in adaptive curve from K = $^{1}/_{16}$ to K = $^{1}/_{8}$; weight of 1
	4 to 7	Kstep1	3	step in adaptive curve from K = $^{1}/_{8}$ to K = $^{2}/_{8}$; weight of 1
21H	0 to 3	Kstep2	4	step in adaptive curve from K = $^{2}/_{8}$ to K = $^{3}/_{8}$; weight of 2
	4 to 7	Kstep3	6	step in adaptive curve from K = $^{3}/_{8}$ to K = $^{4}/_{8}$; weight of 2
22H	0 to 3	Kstep4	4	step in adaptive curve from K = $^{4}/_{8}$ to K = $^{5}/_{8}$; weight of 4
	4 to 7	Kstep5	6	step in adaptive curve from K = $^{5}/_{8}$ to K = $^{6}/_{8}$; weight of 4
23H	0 to 3	Kstep6	4	step in adaptive curve from K = $^{6}/_{8}$ to K = $^{7}/_{8}$; weight of 8
	4 to 7	Kstep7	6	step in adaptive curve from K = $^{7}/_{8}$ to K = $^{8}/_{8}$; weight of 8
Subregister 24H (K-factor controls of luminance)				
24H	0 to 3	Klumafix	15	value of the fixed K-factor of the luminance; see Table 3
	4 to 6	Yadapt_gain	1	value of the gain of the adaptive curve of the luminance; see Table 2
	7	lumafix	0	adaptive (lumafix = 0) or fixed K mode (lumafix = 1) of the luminance
Subregister 25H (K-factor controls of chrominance)				
25H	0 to 3	Kchromafix	15	value of the fixed K-factor of the luminance; see Table 3
	4 to 6	Cadapt_gain	1	value of the gain of the adaptive curve of the chrominance; see Table 2
	7	chromafix	0	adaptive (chromafix = 0) or fixed K mode (chromafix = 1) of chrominance
Subregister 26H (miscellaneous)				
26H	0	DPCMin	0	if HIGH: converts the chrominance input from DPCM to 4 : 2 : 2 format
	1	DPCMout	0	if HIGH: converts the chrominance output from 4 : 2 : 2 to DPCM format
	2	Klumatochroma	0	if HIGH: uses luminance K-factor for chrominance path
	3	unfiltered	0	if HIGH: band splitting is deactivated, complete difference signals are used
	4	noise_shape	1	if HIGH: noise shaping is activated
	5	chroma_invert	0	if HIGH: chrominance input signals U and V are inverted
	6	split_screen	0	if HIGH: demo mode is activated with noise reduction only at the right screen side
	7	reserved		
Subregister 27H (miscellaneous)				
27H	0	no_refresh	0	if HIGH: disables internal self-refresh to allow $T_{cy(SWCK)}$ = 29 ns for PAN-IC
	1	field_sync	0	if HIGH: synchronizes the noise reduction via RSTW (split_screen and DPCM not possible). Otherwise sync is line related detected by WE 5 cycle LOW followed by a HIGH cycle.
	2 to 7	reserved		

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 19)		–0.5	+5	V
$V_{DD(O)}$	supply voltage (pin 22)		–0.5	+5	V
$V_{DD(P)}$	supply voltage for protection circuits		–0.5	+5.5	V
V_I	input voltage	$V_{DD(P)}$ = 5 V	–0.5	+5.5	V
		$V_{DD} = V_{DD(O)} = V_{DD(P)}$ = 3.3 V	–0.5	+3.8	V
V_O	output voltage	$V_{DD(P)}$ = 5 V	–0.5	+5	V
		$V_{DD} = V_{DD(O)} = V_{DD(P)}$ = 3.3 V	–0.5	+3.8	V
$I_{DD(tot)}$	total supply current		–	200	mA
$\Delta V_{GND-OGND}$	voltage difference between GND and OGND		–0.5	+0.5	V
$I_{O(sc)}$	short-circuit output current		–	50	mA
P_{tot}	total power dissipation		–	750	mW
T_{stg}	storage temperature		–20	+150	°C
T_j	junction temperature		0	125	°C
T_{amb}	ambient temperature		0	70	°C
V_{es}	electrostatic handling	note 1	–200	+200	V
		note 2	–2000	+2000	V

Notes

1. Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (‘0 Ω’ is actually 0.75 μH + 10 Ω).
2. Human body model: equivalent to discharging a 100 pF capacitor through a 1500 Ω series resistor.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	60	K/W

10 CHARACTERISTICS

V_{DD} = $V_{DD(O)}$ = $V_{DD(P)}$ = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; 3 ns input transition times; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage (pin 19)		3.0	3.3	3.6	V
$V_{DD(O)}$	supply voltage (pin 22)		3.0	3.3	3.6	V
$V_{DD(P)}$	supply voltage (pin 21)		3.0	3.3	5.5	V
$I_{DD(tot)}$	total supply current ($I_{DD(tot)}$ = I_{DD} + $I_{DD(O)}$ + $I_{DD(P)}$)	minimum write/read cycle; outputs open-circuit	–	27	70	mA
I_{DD}	operating supply current	minimum write/read cycle	–	25	60	mA
$I_{DD(std)}$	stand-by supply current	after 1 RSTW/RSTR cycle; NREN, WE, RE and OE = LOW	–	3	10	mA
$I_{DD(O)}$	supply current	minimum write/read cycle; outputs open-circuit	–	2	10	mA
$I_{DD(P)}$	supply current		–	0	1	mA
Inputs except I²C-bus signals (pins 3 to 18, 23 to 26 and 40)						
V_{IH}	HIGH-level input voltage		2.0	–	$V_{DD(P)}$ + 0.3	V
V_{IL}	LOW-level input voltage		–0.5	–	+0.8	V
I_{LI}	input leakage current	V_i = 0 V to $V_{DD(P)}$	–10	–	+10	µA
C_i	input capacitance	f = 1 MHz; V_i = 0 V	–	–	7	pF
Inputs of I²C-bus signals: SCL (pin 1) and SDA (pin 20); note 2						
V_{IH}	HIGH-level input voltage		3.0	–	$V_{DD(P)}$ + 0.5	V
V_{IL}	LOW-level input voltage		–0.5	–	+1.5	V
I_{LI}	input leakage current	V_i = 0 V to $V_{DD(P)}$	–10	–	+10	µA
C_i	input capacitance	f = 1 MHz; V_i = 0 V	–	–	10	pF
Outputs except I²C-bus signal SCL (pins 27 to 38)						
V_{OH}	HIGH-level output voltage	I_{OH} = –5 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4.2 mA	–	–	0.4	V
I_{LO}	output leakage current		–10	–	+10	µA
C_o	output capacitance	f = 1 MHz; V_o = 0 V	–	–	10	pF
Output of I²C-bus signal: SDA (pin 20); note 2						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.4	V
I_{LO}	output leakage current		–10	–	+10	µA
C_o	output capacitance	f = 1 MHz; V_o = 0 V	–	–	10	pF
Write cycle timing; note 3						
$T_{cy(SWCK)}$	SWCK cycle time	NREN = LOW; see Fig.4	26	–	–	ns
		NREN = HIGH; see Fig.4	52	–	150	ns
$t_{W(SWCKH)}$	SWCK HIGH pulse width	see Fig.4	7	–	–	ns
$t_{W(SWCKL)}$	SWCK LOW pulse width	see Fig.4	7	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
$t_{su(D)}$	set-up time data inputs (D0 to D11)	see Fig.4	5	–	–	ns
$t_{h(D)}$	hold time data inputs (D0 to D11)	see Fig.4	3	–	–	ns
$t_{su(RSTW)}$	set-up time RSTW	see Fig.4	5	–	–	ns
$t_{h(RSTW)}$	hold time RSTW	see Fig.4	3	–	–	ns
$t_{su(WE)}$	set-up time WE	see Fig.8	5	–	–	ns
$t_{h(WE)}$	hold time WE	see Fig.8	3	–	–	ns
$t_{W(WEL)}$	WE LOW pulse width	see Fig.8	8	–	–	ns
$t_{su(IE)}$	set-up time IE	see Fig.9	5	–	–	ns
$t_{h(IE)}$	hold time IE	see Fig.9	3	–	–	ns
$t_{W(IEL)}$	IE LOW pulse width	see Fig.9	8	–	–	ns
t_t	transition time (rise and fall)	see Fig.4	–	3	30	ns
Read cycle timing; note 4						
t_{ACC}	access time after SRCK	see Fig.11	–	–	21	ns
$t_{en(Q)}$	output enable time after SRCK	see Fig.15	–	–	21	ns
$t_{dis(Q)}$	output disable time after SRCK	note 5; see Fig.15	–	–	12	ns
$t_{h(Q)}$	output hold time after SRCK	see Fig.11	3	–	–	ns
$T_{cy(SRCK)}$	SRCK cycle time	see Fig.11	26	–	–	ns
$t_{W(SRCKH)}$	HIGH-level pulse width of SRCK	see Fig.11	7	–	–	ns
$t_{W(SRCKL)}$	LOW-level pulse width of SRCK	see Fig.11	7	–	–	ns
$t_{su(RSTR)}$	set-up time RSTR	see Fig.11	5	–	–	ns
$t_{h(RSTR)}$	hold time RSTR	see Fig.11	3	–	–	ns
$t_{su(RE)}$	set-up time RE	see Fig.14	5	–	–	ns
$t_{h(RE)}$	hold time RE	see Fig.14	3	–	–	ns
$t_{W(REL)}$	LOW-level pulse width of RE	see Fig.14	9	–	–	ns
$t_{su(OE)}$	set-up time OE	see Fig.15	5	–	–	ns
$t_{h(OE)}$	hold time OE	see Fig.15	3	–	–	ns
$t_{W(OEL)}$	LOW-level pulse width of OE	see Fig.15	9	–	–	ns
t_t	transition time (rise and fall)	see Fig.11	–	3	30	ns

Notes

1. Typical values are valid for T_{amb} = 25 °C, $V_{DD} = V_{DD(O)} = V_{DD(P)}$ = 3.3 V, all voltages referenced to GND. See Fig.1 for configuration.
2. The AC characteristics are in accordance with the I²C-bus specification for fast mode (clock frequency maximum 400 kHz). Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011).
3. The write cycle timing set-up and hold times are related to V_{IL} of the rising edge of SWCK. They are valid for the specified LOW and HIGH-level input voltages (V_{IL} and V_{IH}).
4. The read cycle timing set-up and hold times are related to V_{IL} of the rising edge of SRCK. They are valid for the specified LOW and HIGH-level input voltages (V_{IL} and V_{IH}). The load on each output is a 30 pF capacitor to ground in parallel with a 218 Ω resistor to 1.31 V.
5. Disable times specified are from the initiating edge until the output is no longer driven by the memory. Disable times are measured by observing the output waveforms. Low values of load resistor and capacitor have to be used to obtain a short time constant.

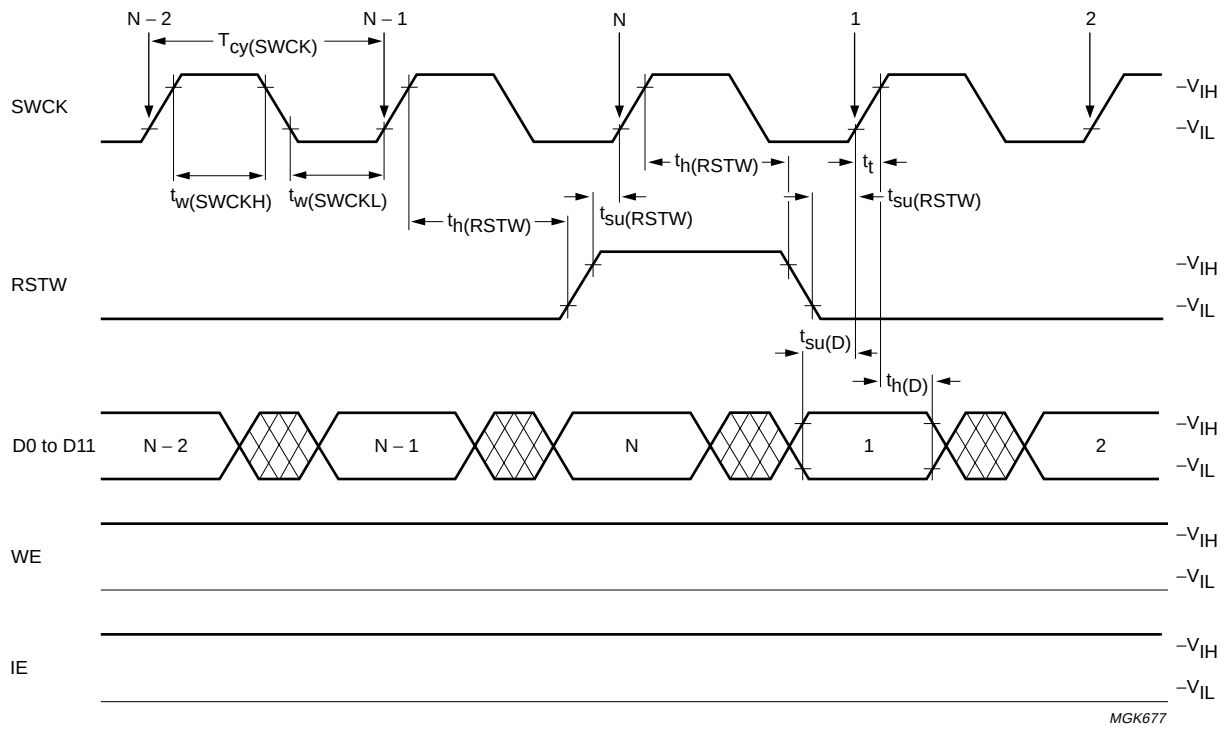


Fig.4 Write cycle timing diagram (reset write).

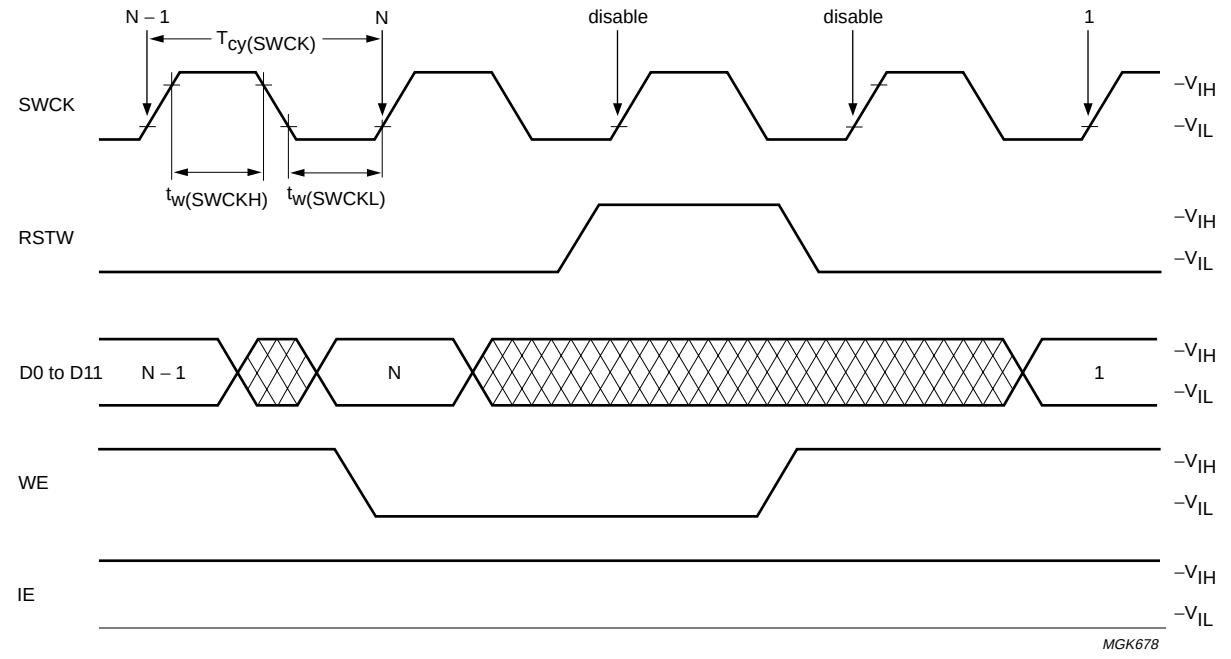


Fig.5 Write cycle timing diagram (reset write with WE LOW).

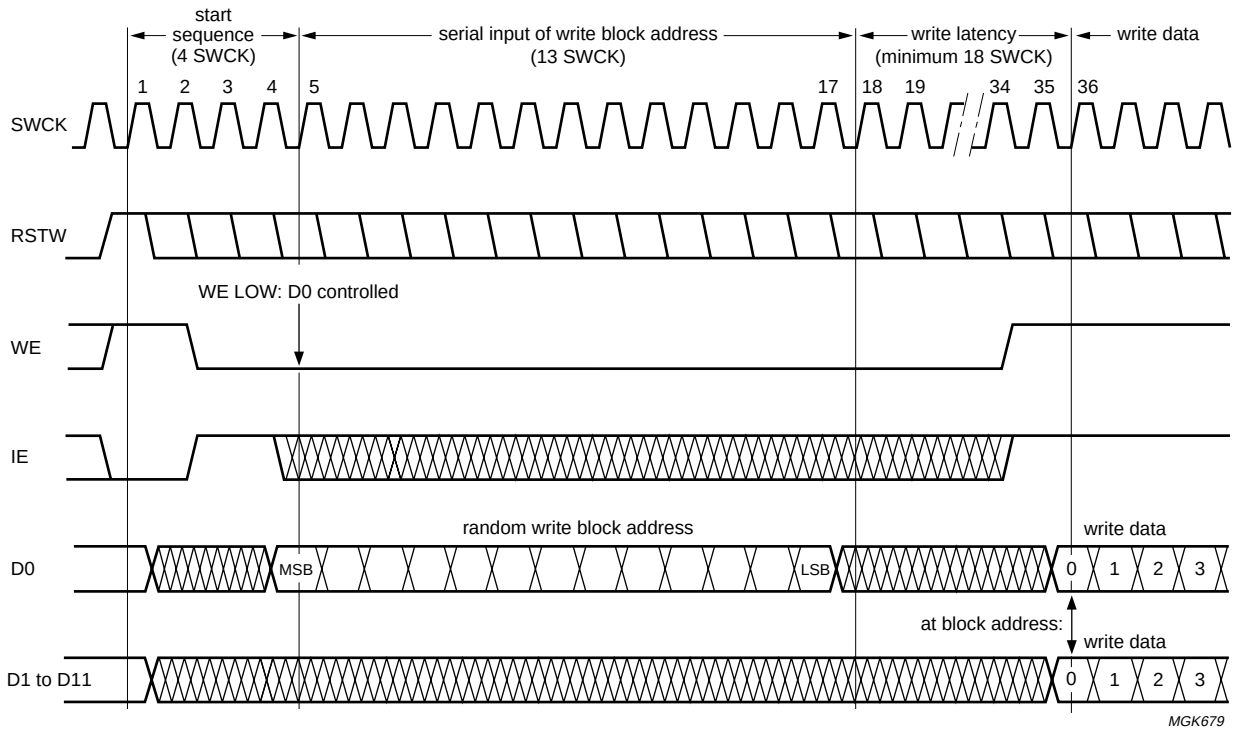


Fig.6 D0 controlled entry sequence of the random write block access mode.

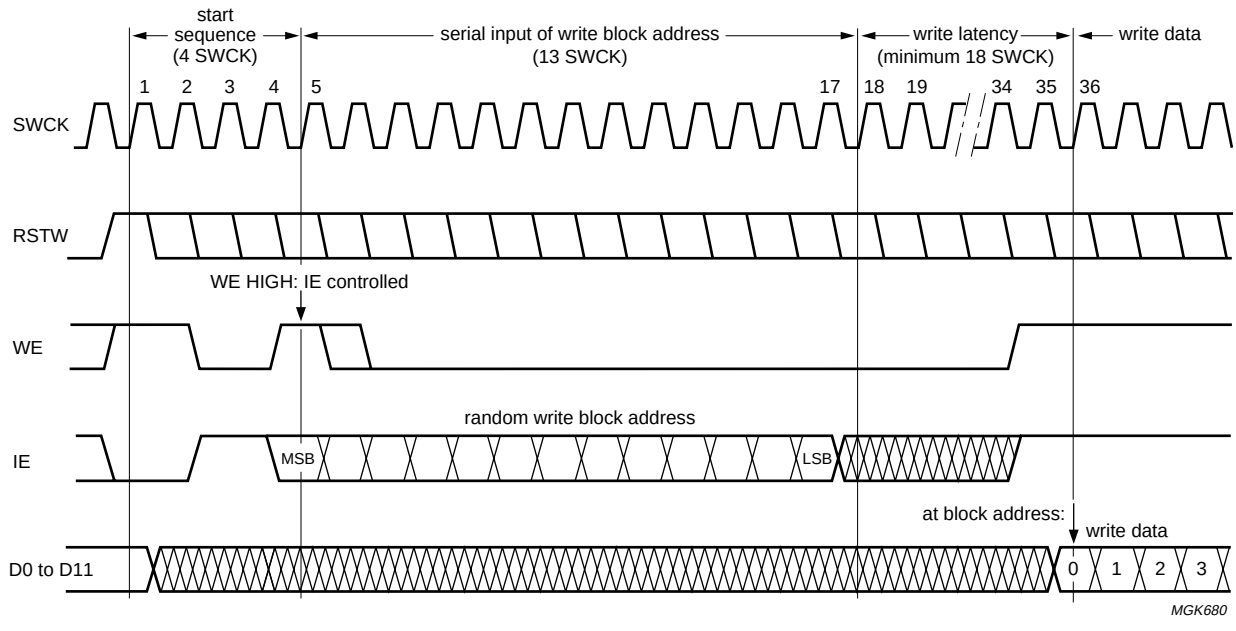


Fig.7 IE controlled entry sequence of the random write block access mode.

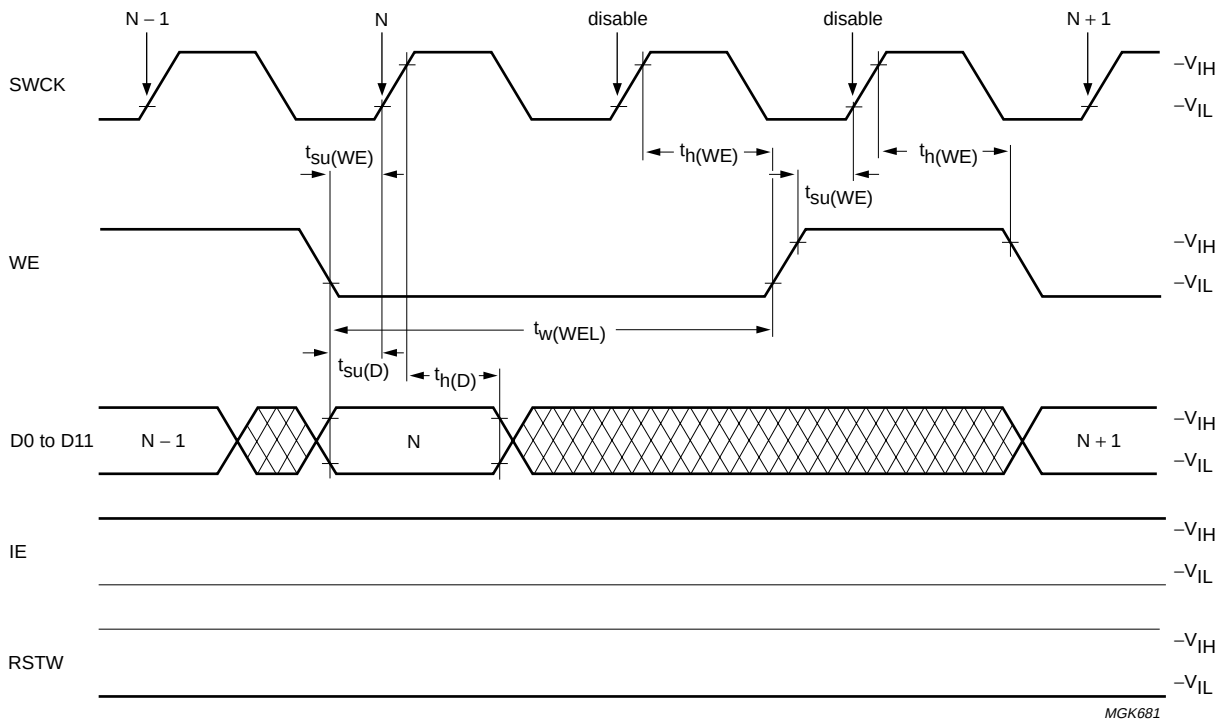


Fig.8 Write cycle timing diagram (write enable).

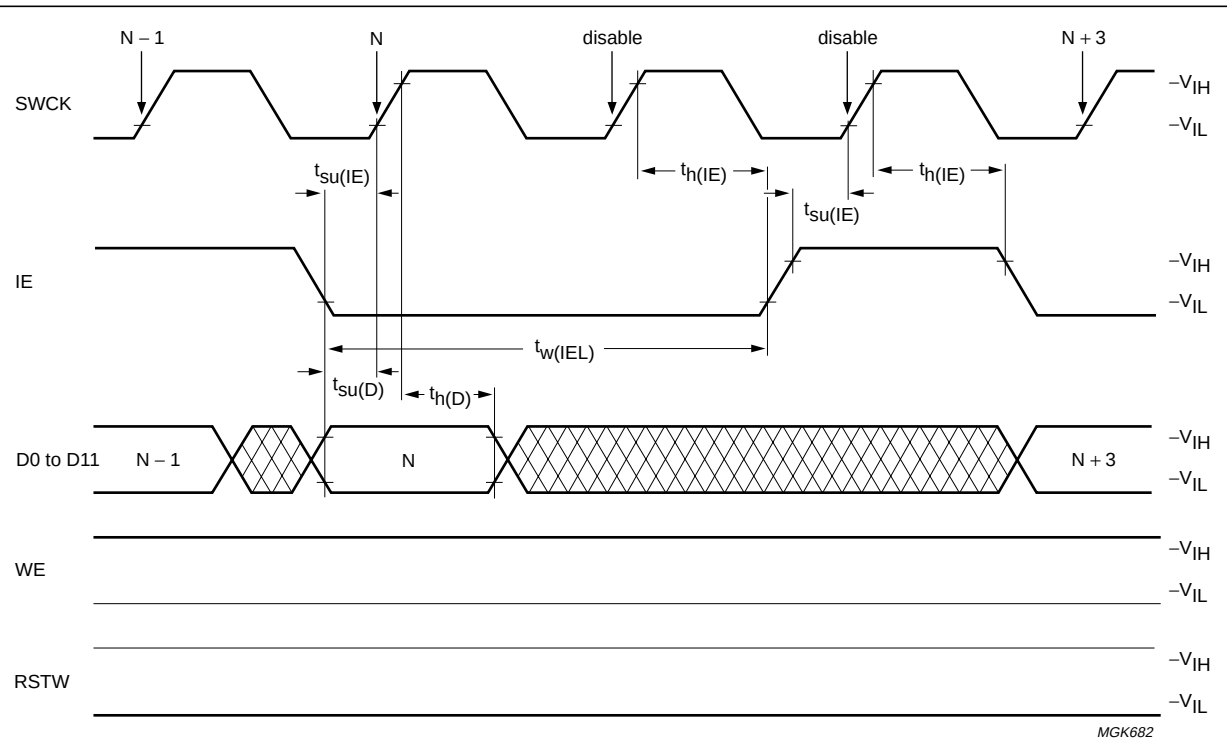


Fig.9 Write cycle timing diagram (input enable = write mask operation).

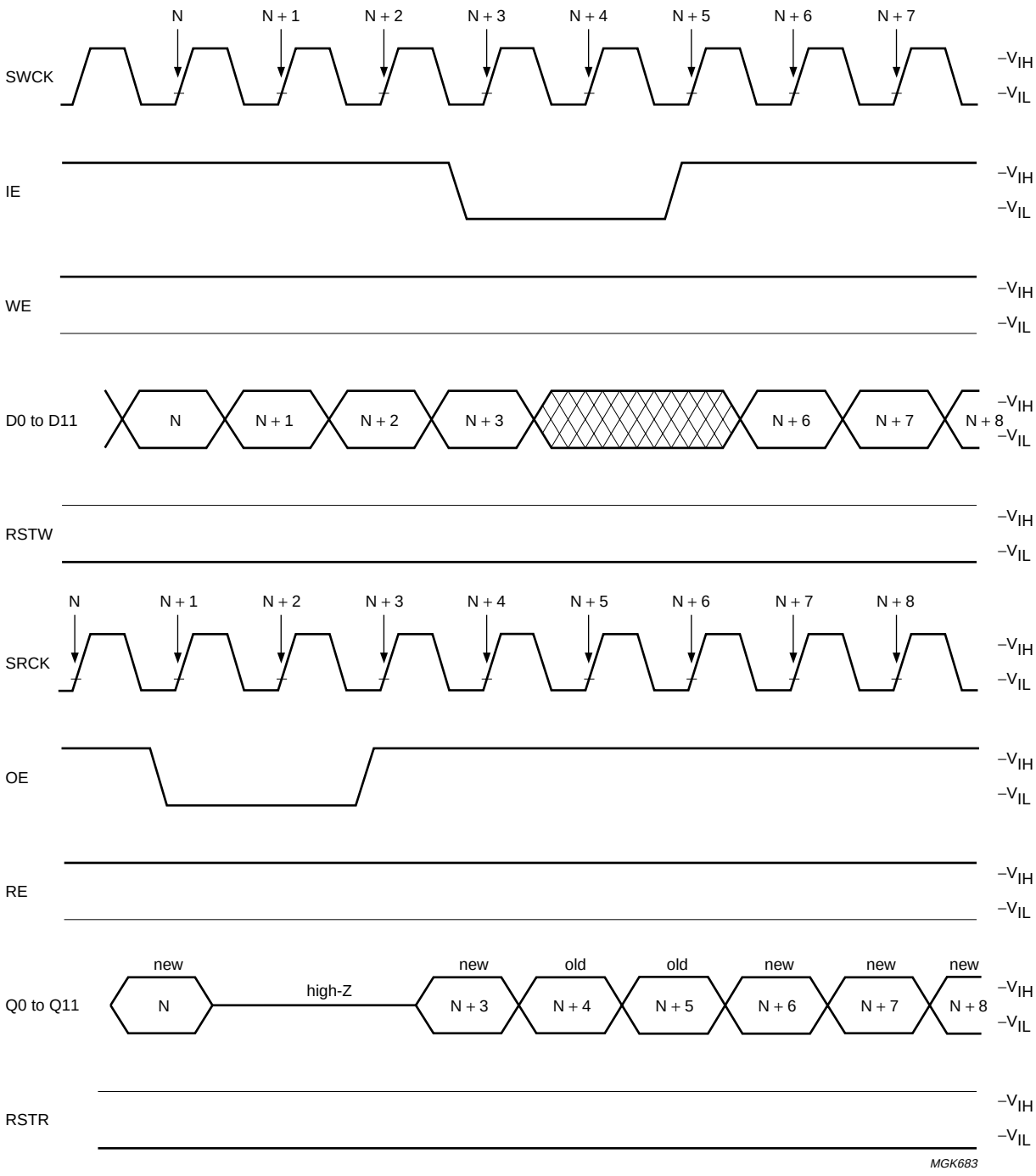


Fig.10 Write mask operation.

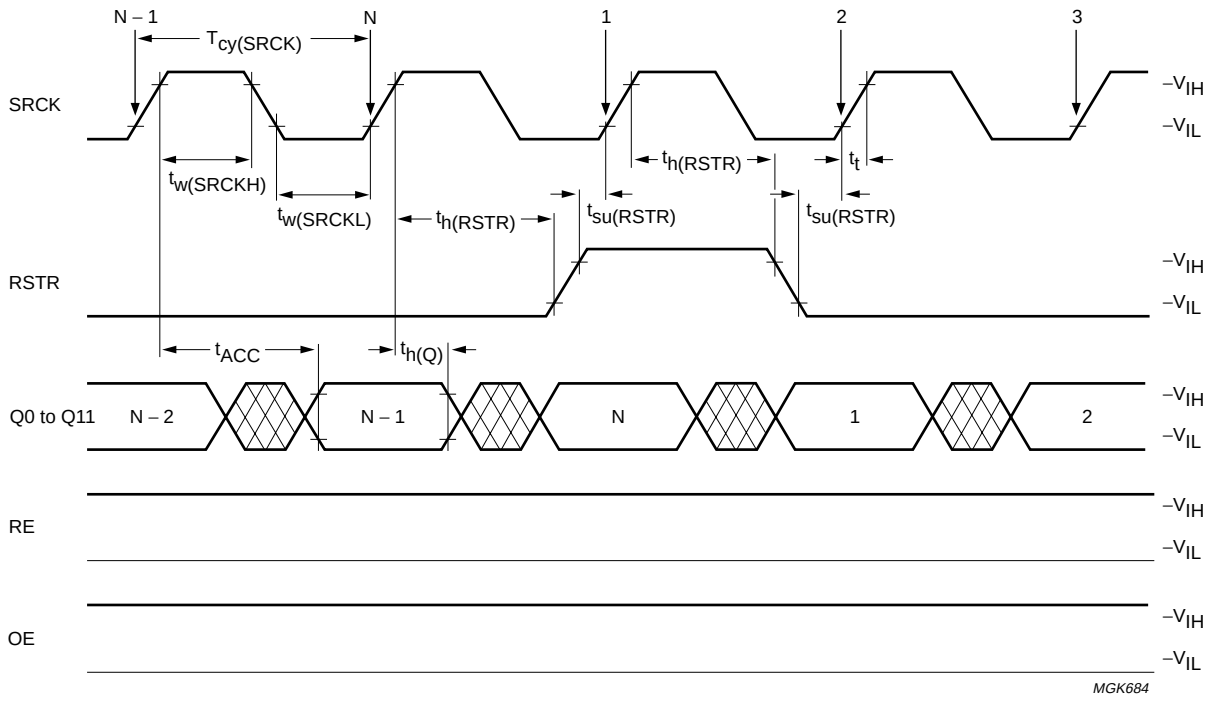


Fig.11 Read cycle timing diagram (reset read).

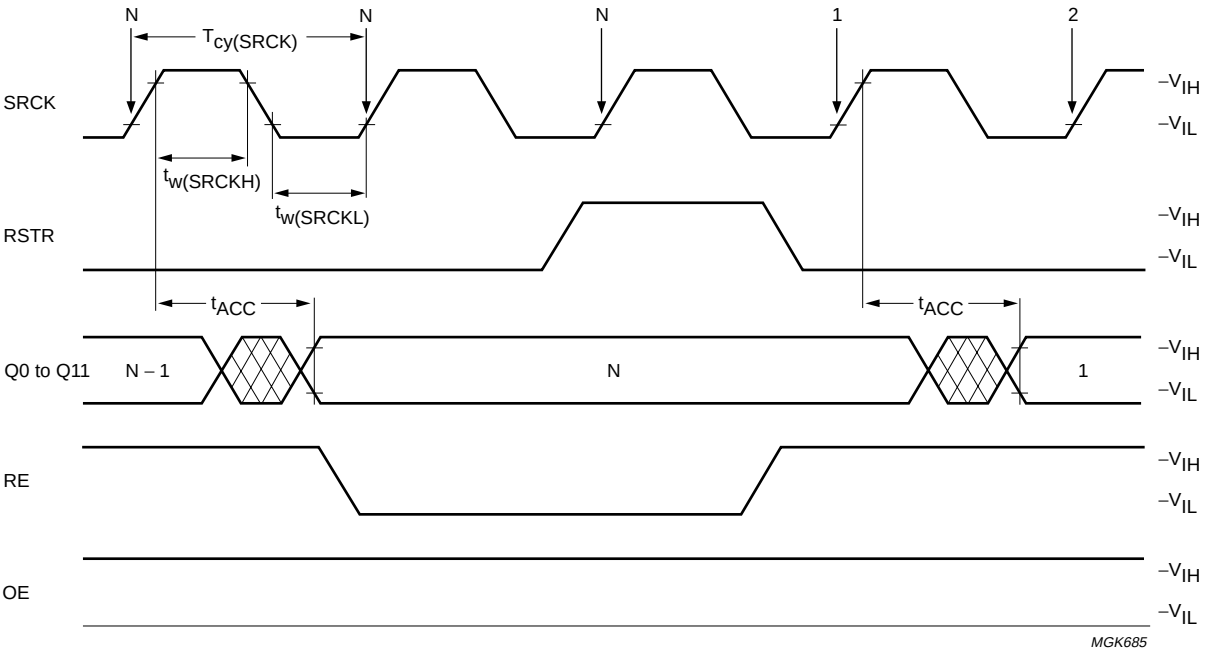


Fig.12 Read cycle timing diagram (reset read with RE LOW).

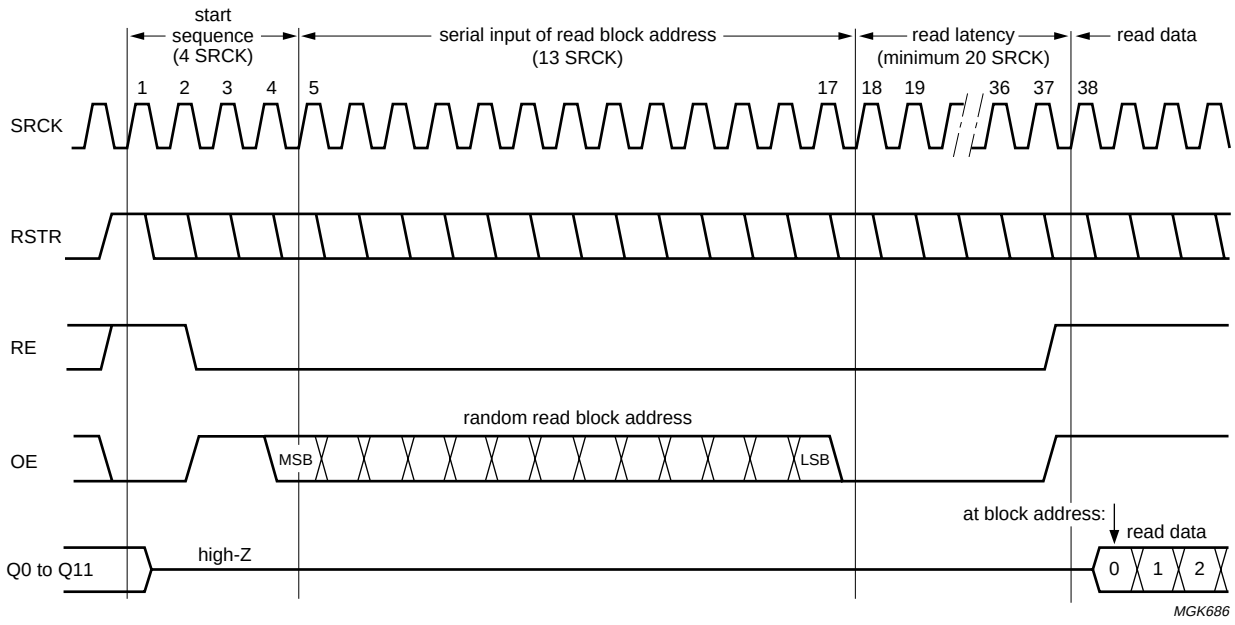


Fig.13 Entry sequence of the random read block access mode.

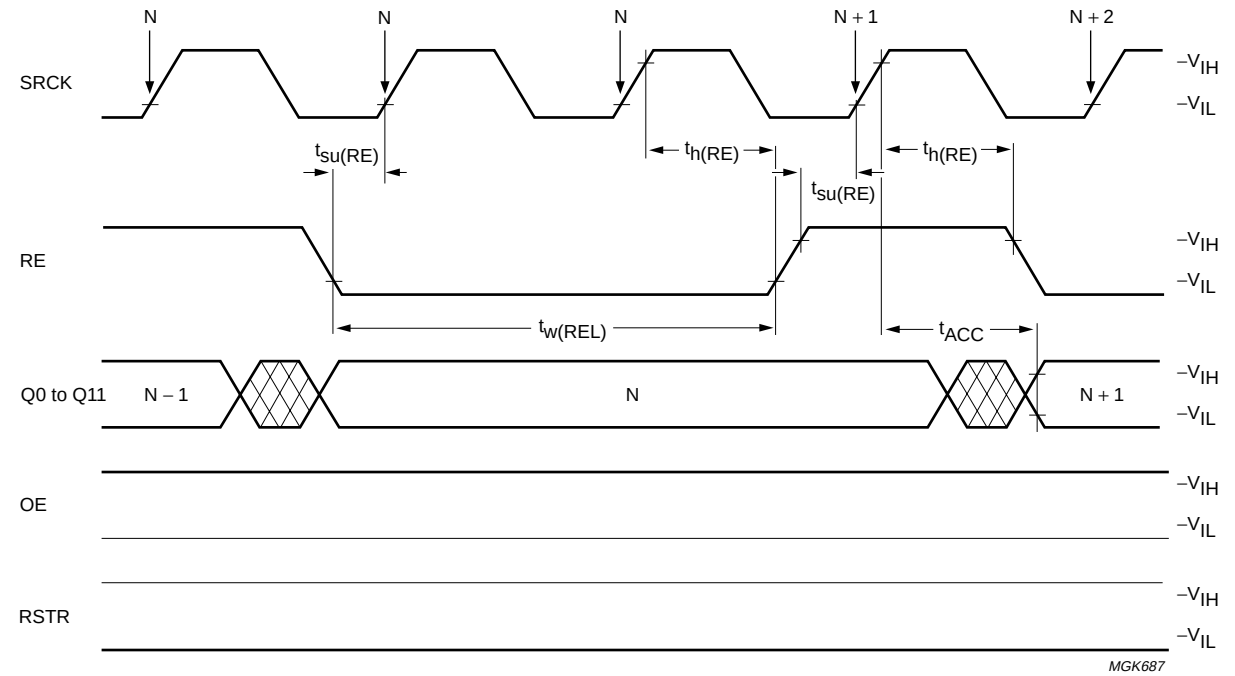


Fig.14 Read cycle timing diagram (read enable).

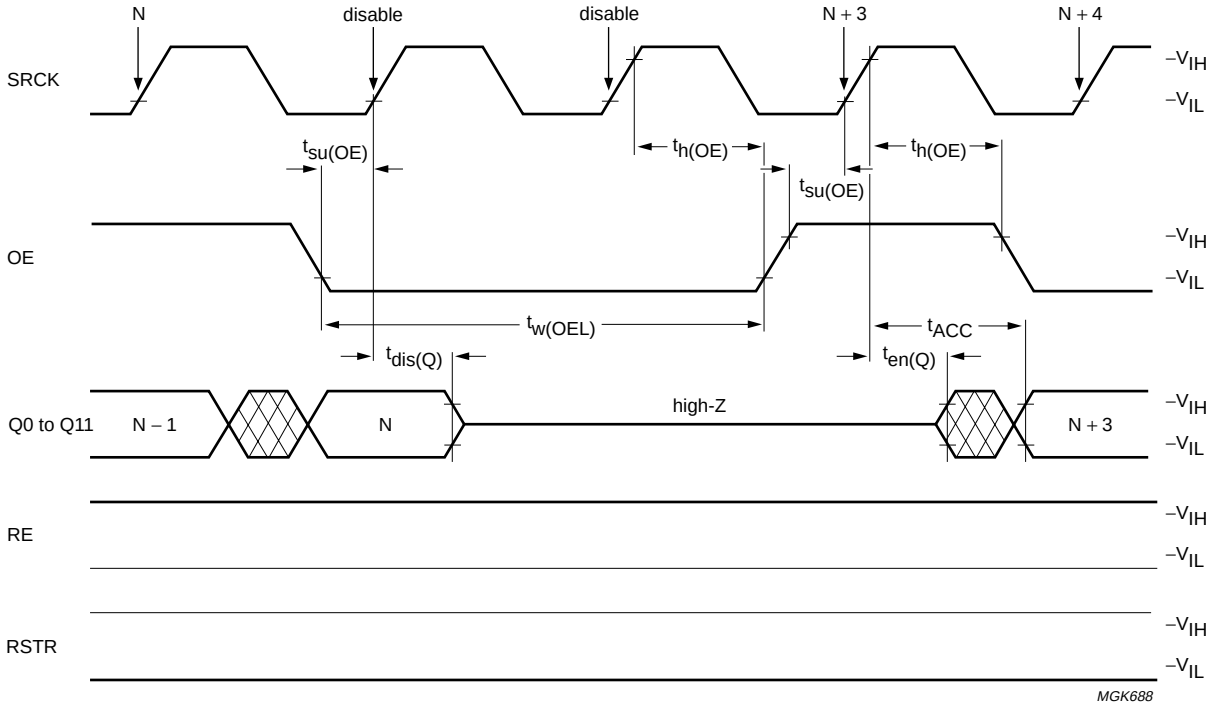


Fig.15 Read cycle timing diagram (output enable).

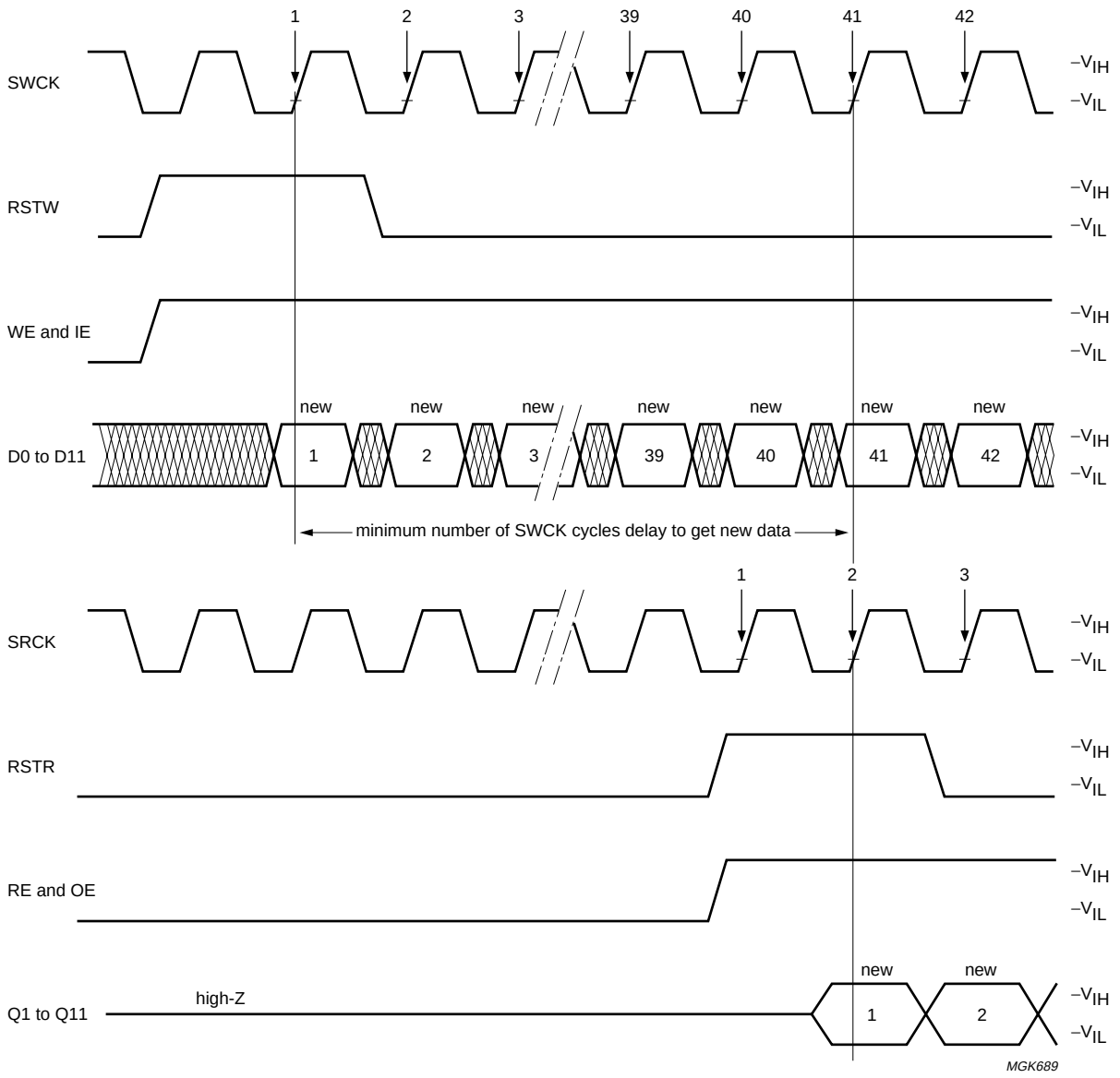


Fig.16 New data access.

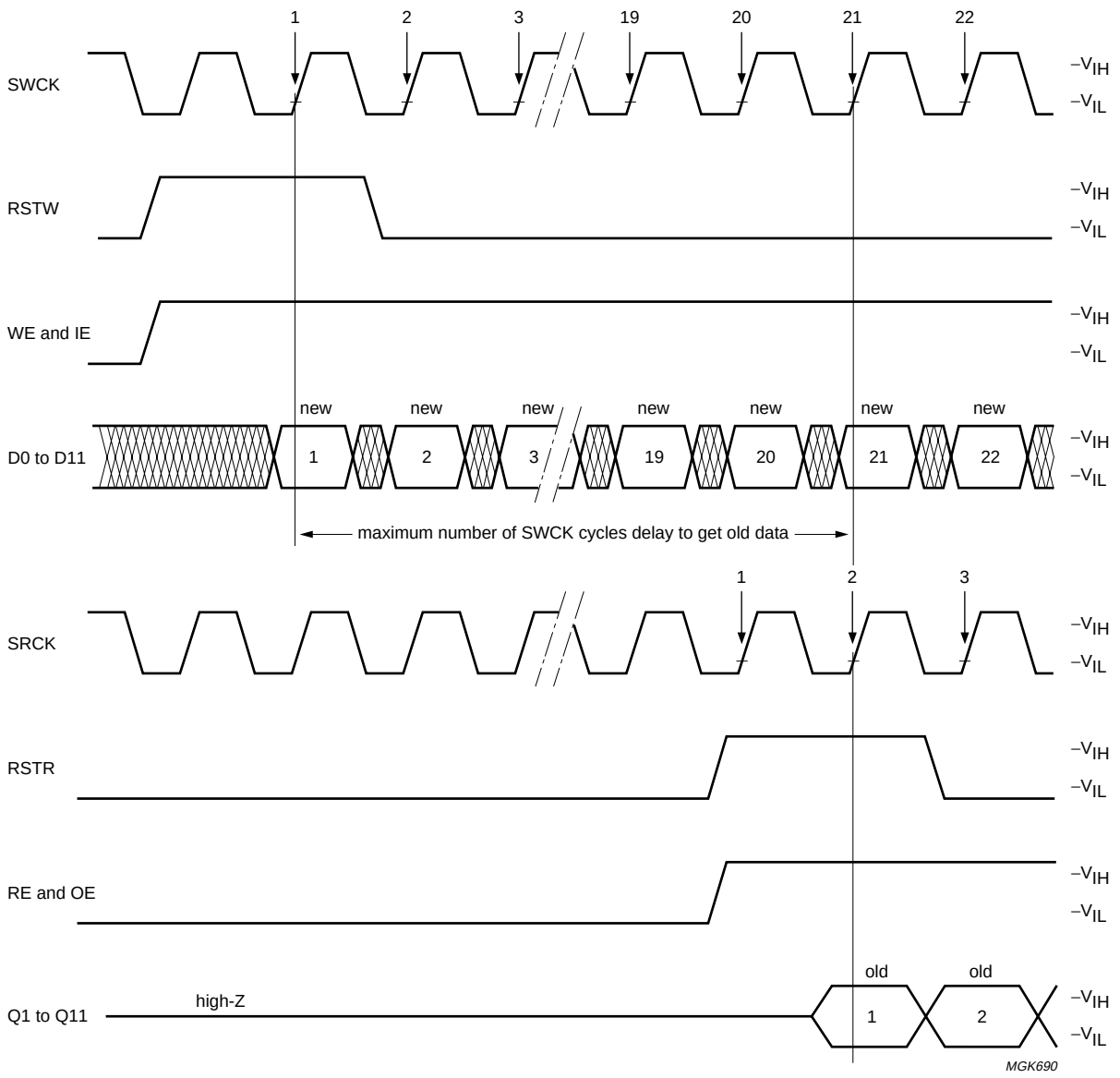


Fig.17 Old data access.

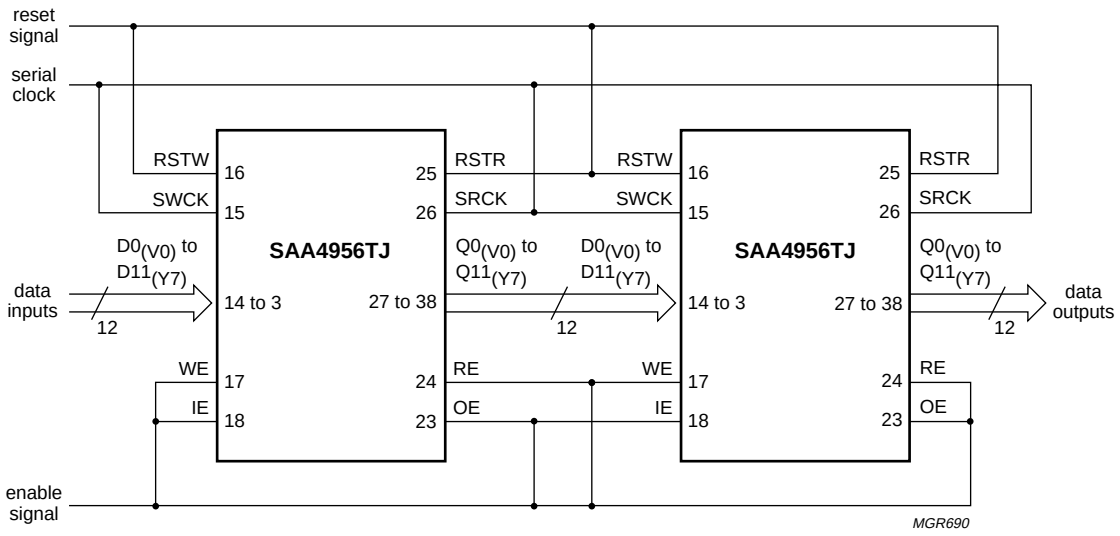


Fig.18 Cascade operation (signal connections).

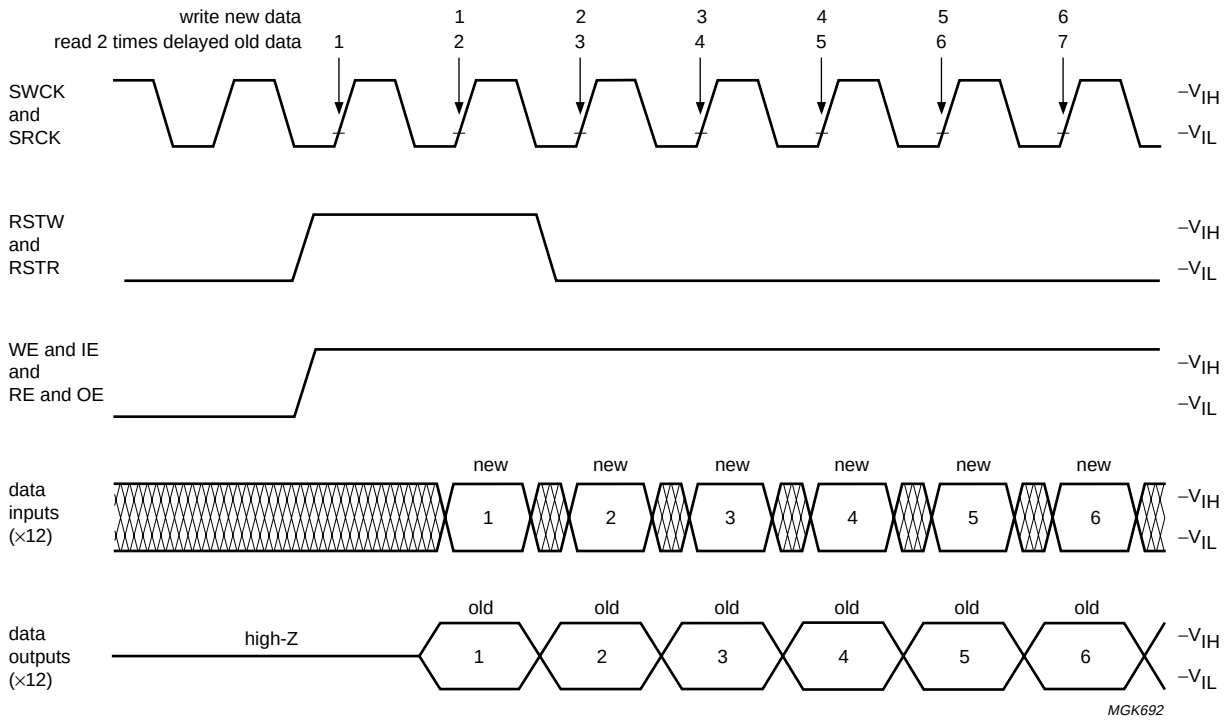


Fig.19 Cascade operation (timing waveforms).

11 APPLICATION INFORMATION

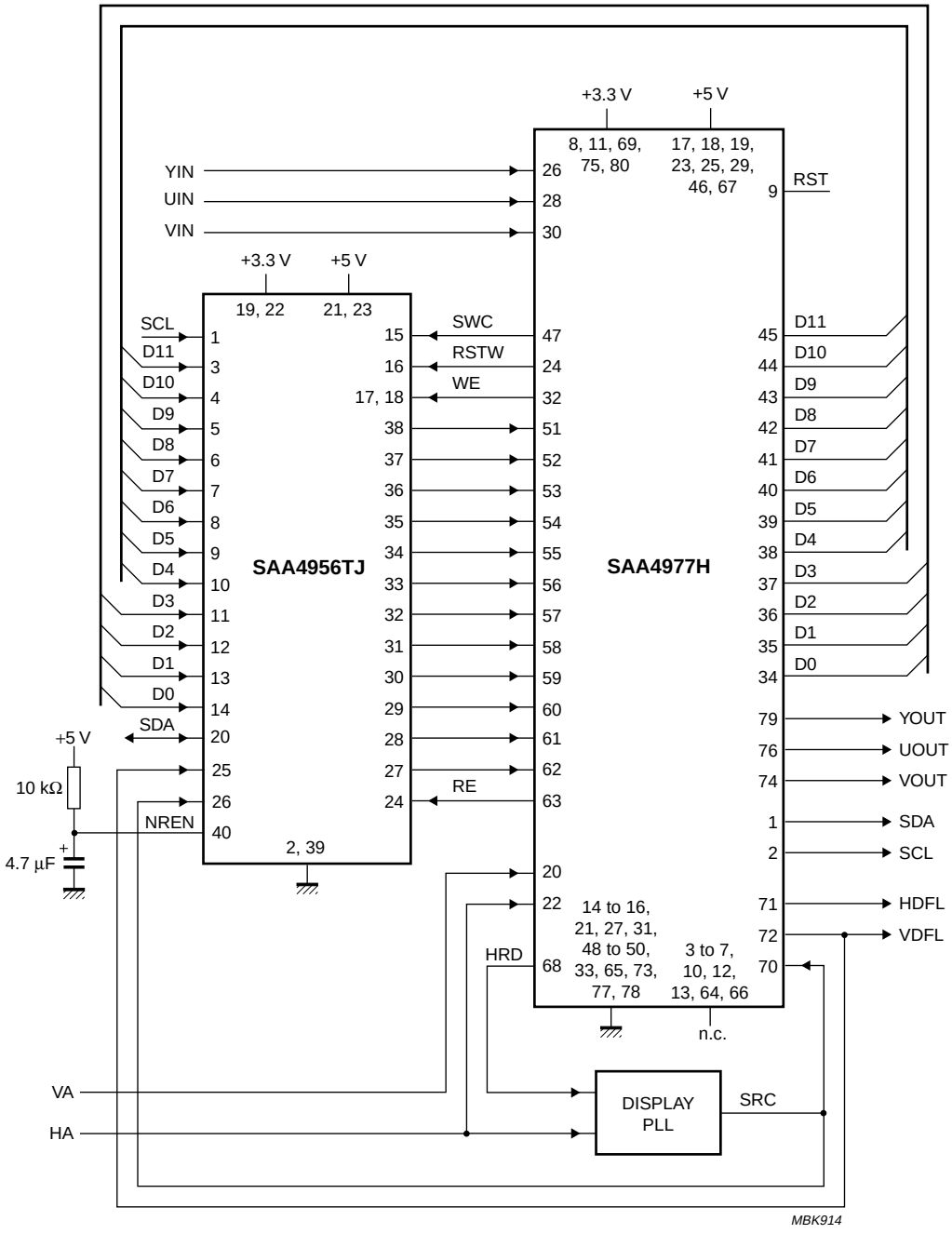
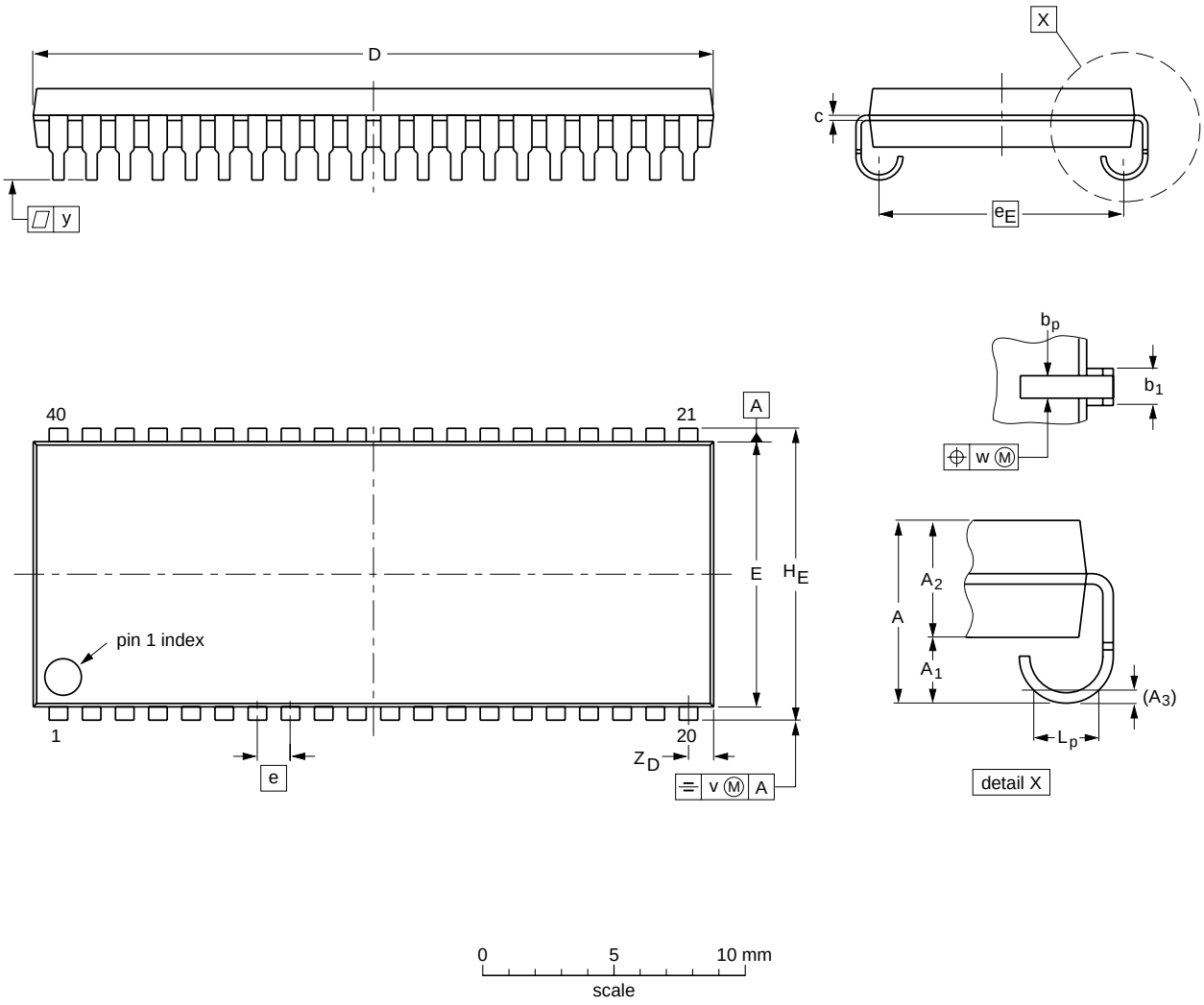


Fig.20 Application diagram.

12 PACKAGE OUTLINE

SOJ40: plastic small outline package; 40 leads (J-bent); body width 10.16 mm **SOT449-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_E	H_E	L_p	v	w	y	$Z_D^{(1)}$
mm	3.68	1.40 1.14	2.29 2.18	0.25	0.51 0.38	0.81 0.66	0.32 0.18	26.2 25.9	10.3 10.0	1.27	9.4	11.30 11.05	1.4 1.1	0.18	0.18	0.1	1.19 0.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT449-1		MS027				97-06-02

13 SOLDERING

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

14 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

15 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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